AMENDMENTS TO THE SPECIFICATION

- Please amend the Title which begins on page 1, line 1, as follows:

~~CMP PROCESSED INTERCONNECT CAP IN INTEGRATED CIRCUITS~~**METHOD OF MANUFACTURING AN INTEGRATED CIRCUIT WITH LOW SOLIBILITY METAL-CONDUCTOR INTERCONNECT CAP**

- Please amend the Cross-Reference to Related Application(s) section, which begins on page 1, line 3, as follows:

CROSS-REFERENCE TO RELATED APPLICATION(S)

This is a divisional application of co-pending application serial number: 10/016,024, filed December 12, 2002, which ~~This application~~ claims the benefit of U.S. Provisional patent application serial number 60/256,419 filed December 18, 2000.

- Please amend the Disclosure of the Invention section, which begins on page 4, line 21, as follows:

DISCLOSURE OF THE INVENTION

~~The present invention provides an integrated circuit having a silicon substrate with a semiconductor device. A device oxide layer is on the silicon substrate and has an opening provided therein. A barrier layer lines the opening, with a seed layer lining the barrier layer, and a conductor core fills the opening over the seed layer. A low solubility metal conductor interconnect cap is disposed over the conductor core and seed layer and is capped with a~~

~~capping layer. The interconnect cap is preferably of a copper-cerium alloy to prevent diffusion through the capping layer.~~

The present invention ~~further~~ provides a method of manufacturing an integrated circuit having a semiconductor substrate with a semiconductor device provided thereon. A dielectric layer is formed on the semiconductor substrate and a channel layer is formed on the dielectric layer with an opening formed therein. A barrier layer, with a seed layer deposited thereon, is deposited to line the channel opening. A conductor core is deposited to fill the channel opening, and is chemically-mechanically polished with the seed layer, barrier layer and dielectric layer. Thermal treatment of the low solubility metal after the chemical-mechanical polishing is performed causes alloying with the conductor in the conductor core to form a low solubility metal-conductor interconnect cap and a capping layer is formed over the dielectric layer and conductor interconnect cap. The interconnect cap is preferably of a copper-cerium alloy to prevent diffusion through the capping layer.

The above and additional advantages of the present invention will become apparent to those skilled in the art from a reading of the following detailed description when taken in conjunction with the accompanying drawings.

- Please amend the Abstract which begins on page 14, line 1, as follows which begins on the next page: